RADCELF

TRIPLE-DDS RADAR SIGNAL GENERATOR
Product Specification

High Performance Simultaneous Data Acquisition

Table of Contents

1 Product Description

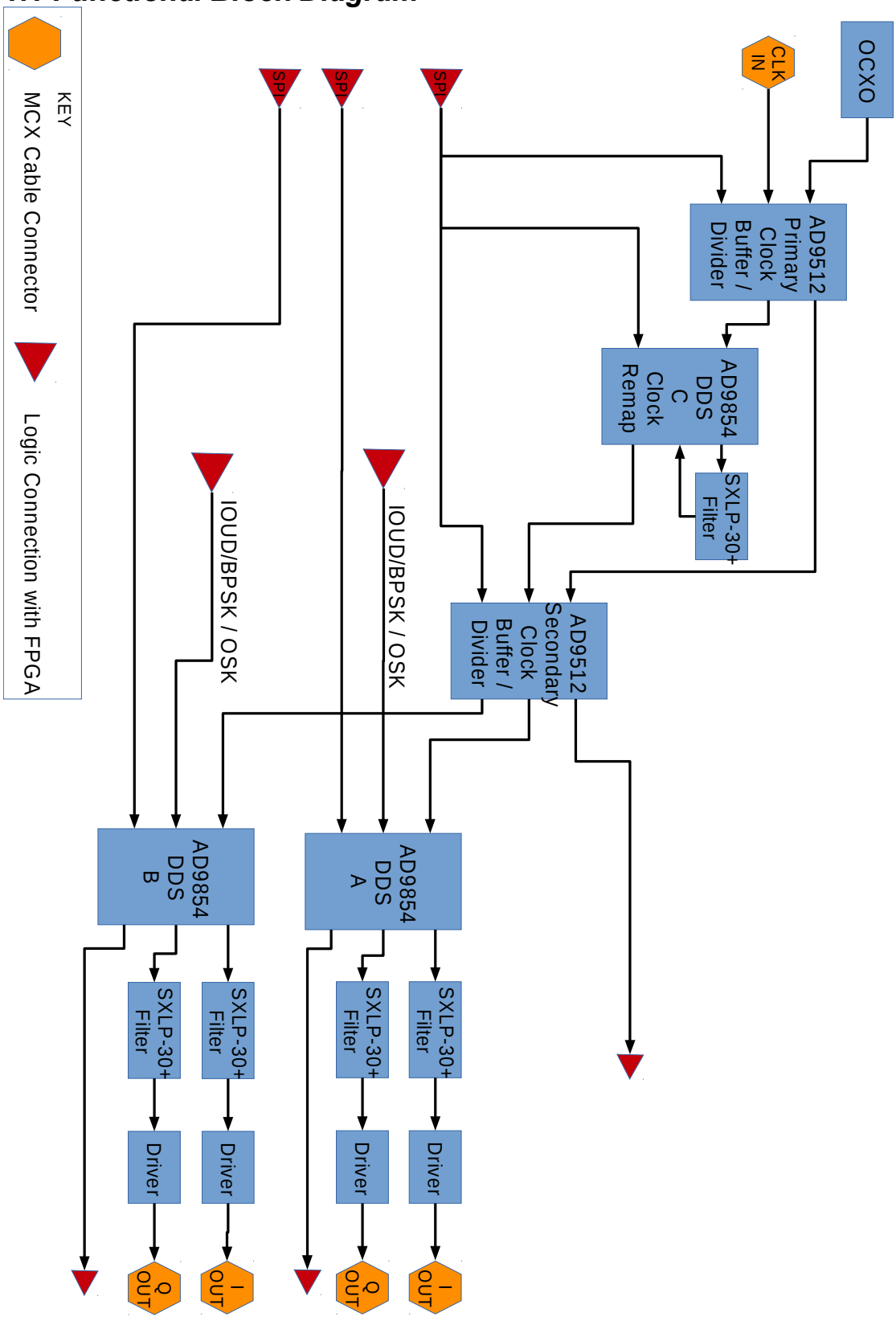
1. RADCELF is a complete clocking system suitable for HF RADAR
2. Circuit board forms the top layer of a 3-layer stack comprising
    1. ACQ1001Q base unit with ZYNQ FPGA
    2. ACQ435ELF digitizer module with 16 or 32 simultaneous AI.
    3. RADCELF
3. Includes 3 x AD9854 DDS devices
    1. ddsA : I+Q outputs, for main system control.
    2. ddsB : I+Q outputs for system calibration.
    3. ddsC : I output for clock remapping
4. Includes 2 x AD9512 CLKD Clock divider/buffer devices
    1. clkdA : Select Oven Local Oscillator or CLK-IN
    2. clkdB : Select Clock source for ddsA, ddsB.
5. All 5 devices are controlled from SPI from the ACQ1001. Multiple SPI channels are used to potentially provide simultaneous register update.
6. Key signal inputs to DDS are provided from the FPGA. All output clocks feed back to the FPGA for monitoring.
7. Provision for Oven Local Oscillator (power supply, socket and space for thermal management) or external clock
8. Signal inputs and outputs on MCX connectors. ddsA, ddsB TRG inputs.
9. Outputs optionally filtered by Minicircuits SXLP filters.
10. I/O expansion:
    1. P18: PMOD connector. (12 pin header with FPGA IO)
    2. J1: VMON (16 pin header, 8 x slow ADC channels, 1Hz, 10bit)
    3. J2: DIO (16 pin header, 8 slow DIO)
    4. USB 2.0, type A port, suitable for USB stick or remote devices.

RADCELF?

RAD : Radar

CELF : “Carrier Elf”, D-TACQ definition for 3 layer stacking board.

1.1 Functional Block Diagram



1.2 Product Variants

- ***RADCELF3*** : 3 x DDS
- ***RADCELF2*** : 2 x DDS (MOQ 20).
- SXLP filters are assumed to be either No Fit or free issue from customer

1.3 Applications

- High speed control and diagnostics.

1.4 Overview

RADCELF forms part of a complete working 32 channel digitizer appliance with Ethernet control. The appliance includes a full Linux OS with full virtual memory support. The DDS and CLKD

For IO expansion, additional ACQ1002S stacks may be daisy chained on the clock trigger highway, for expansion from 32 to 64, 96 and more simultaneous analog inputs.

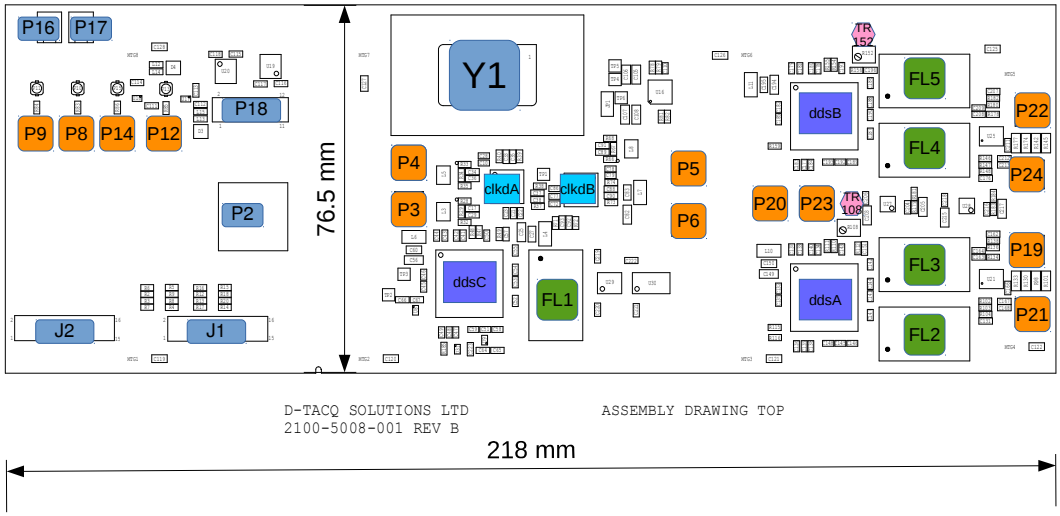
1.5 Glossary

- *FMC*: VITA57 FPGA Mezzanine Card.
- Xilinx ZYNQ Soc
- *FPGA* : Field Programmable Gate Array.
- *LPC* : *FMC* Low pin count wiring standard.
- *ULPC*: *FMC* Ultra low pin count (D-TACQ).
- ULPC+ D-TACQ Ultra low pin count with LVDS
- Extended, ELF : *FMC* Extended size module (D-TACQ).

1.6 References

- RADCELF User Guide.

2 Physical



2.1 Devices

- ddsA, ddsB, ddsC : AD9854 DDS devices
- clkdA, clkdB: AD9513 CLK divider/distributors.
- FL1..FL5 DDS output filters
- Y1 DIL socket for LO
- TR152, TR108 : DDS output level match trimpots.

2.2 MCX Connectors

ID	IO	Description	Opt?
P3	I	EXT CLK INPUT	
P4	O	OCXO LO Monitor	
P5	O	REMAP CLK Monitor	X
P6	O	clkdB Monitor	X
P8	IO	Link tee with uFL P10	X
P9	IO	Link tee with uFL P11	X
P12	IO	DDS A Trigger tee with uFL P13	
P14	IO	DDS B Trigger tee with uFL P15	
P19	O	DDS A I output	
P20	O	DDS A monitor output	X
P21	O	DDS A Q output	
P22	O	DDS B I output	

ID	IO	Description	Opt?
P23	O	DDS B monitor output	X
P24	O	DDS B Q output	

2.2.1 Misc Connectors

ID	Type	Description	Opt?
P2	USB-A	USB 2.0 Master	
P16	2-pin HDR	3V3 external	X
P17	2-pin HDR	5V external	X
P18	12 pin HDR	PMOD Header	
J1	16 pin HDR	AI 8 slow monitor	
J2	16 pin HDR	DIO 8 slow control/monitor	

2.3 RADCELF Dimensions

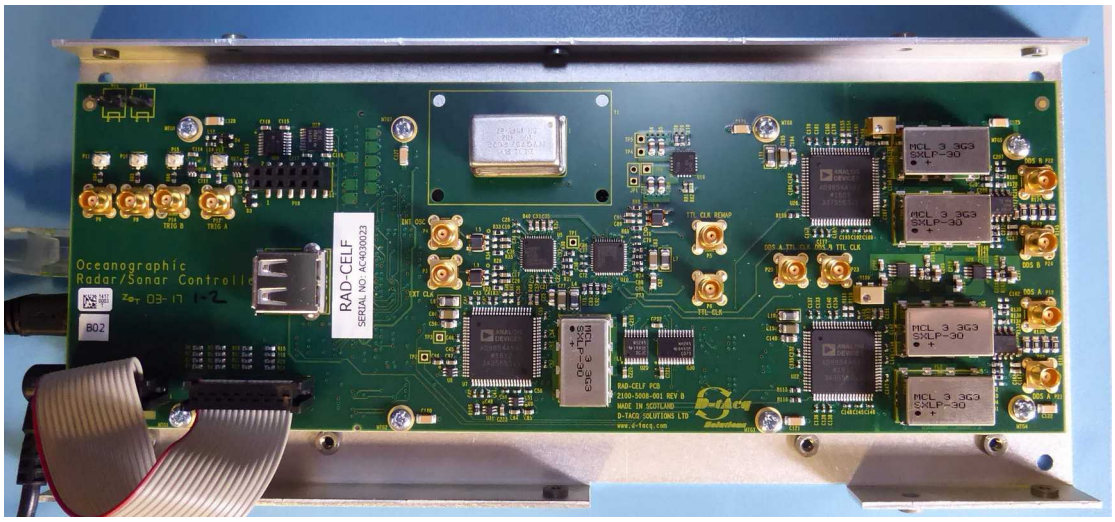
2.3.1 Length 218mm

2.3.2 Width 76.5mm

2.3.3 Stack Height 50mm

2.4 Appearance

2.4.1 Plan View



2.4.2 Side view of Stack up

Top to Bottom:

- RADCELF
- ACQ435ELF : 16/32 channel simultaneous ADC
- ACQ1001: FPGA/Computer control module.
- Customer plinth base.

3 Interface Specification.

3.1 OCXO socket

Standard 14 pin socket is provided for a OCXO.

Linear regulated 5V power at up to 1A (warm up) and 500 mA (steady state)

Sine or Square Wave output 2-7 dBm

Tested with Bliley NV79 .

Physical separation with mounting holes to allow the OCXO to be encased for thermal separation

3.2 I/O Connectors

3.2.1 I& Q Output MCX Connectors

All outputs are a nominal 7dBm output with 50 Ohm impedance

3.2.2 Clock Input

Connector P3 transformer coupled 2-7dBm 50 Ohm input Square or Sine Wave input.

3.2.3 Trigger Inputs

The two trigger input functionality is application dependent. These are 5V TTL compatible inputs with optional output functionality.

3.3 Clock Monitors

P4 allows the oscillator to be monitored it is a direct connection to the output of the OCXO Oscillator

P5 is a TTL output monitor of the square wave frequency of the Clock Remapping DDS – DDS C. This is the square-wave produced by the AD9654 comparator.

P6 is a TTL output monitor of the input Clock to the two main DDS devices DDS A and DDS B. This signal is controlled from the secondary AD9512 device and can therefore be overridden under software control to produce a divide by N output if desired.

P20 and P23 are TTL monitors of the square wave frequency of DDS A and DDS B. This is the square-wave produced by the AD9654 comparator.

3.4 Misc Connectors

3.4.1 P16 3V3 External

Auxiliary 3V3 output 100 mA max.

3.4.2 P17 5V External

Auxiliary 5V output 100 mA max.

3.4.3 P18 PMOD Header

12 pin 0.1” box header socket for use with PMOD modules.

PMOD is a simple low-cost expansion standard.

Using the PMOD requires FPGA customisation depending on PMOD chosen. Please contact D-TACQ with requirements.

PMOD definition

3.4.4 J1 AI 8 Slow monitor

16 pin 0.1” box header plug for monitoring slow AI signals.

Input range: 0..5V, 10 bit conversion, 1Hz typical rate. 20K input impedance.

Access through Linux device driver.

2x LM7417 devices include temperature monitor.

Pin	***Channel***
2	AI1
4	AI2
6	AI3
8	AI4
10	AI5
12	AI6
14	AI7
16	AI8
1,3,5,15	GND

3.4.5 J2 DIO control

16 pin 0.1” box header plug for slow DIO control.

5V TTL. Access through Linux device driver.

Pin	***Channel***
2	DIO1
4	DIO2
6	DIO3
8	DIO4
10	DIO5
12	DIO6
14	DIO7
16	DIO8
1,3,5,15	GND

4 RADCELF Electrical Specification

4.1 DIO Connector

#	Parameter	Value
1	Number of Channels	8
2	Sample Rate	I2C device with 1 Hz typical update
3	I/O Voltage Range	0-5V
4	Input Voltage High	> 4.0V (@ 10mA)
5	Input Voltage Low	< 0.2V (@ 10mA)
6	Input Voltage Withstand	-0.5 to 6.5V
7	Output Current High	-32mA, -100mA max total
8	Output Current Low	32mA, 100mA max total

4.2 Analog Outputs

Both A & B DDS devices drive both I & Q outputs via an output Amplifier of type OPA2694 with a nominal 7dBm drive capability. Potentiometer available on each DDS to set the nominal output amplitude R108 for DDS A and R152 for DDS B

5 RADCELF Specification

#	Parameter	Value
1	Form Factor	D-TACQ CELF
2	Power source	D-TACQ Carrier Only
3	Environmental	0°C-50°C Operational -10°C-85°C Non-Operational
4	Carrier Socket	D-TACQ CELF Socket