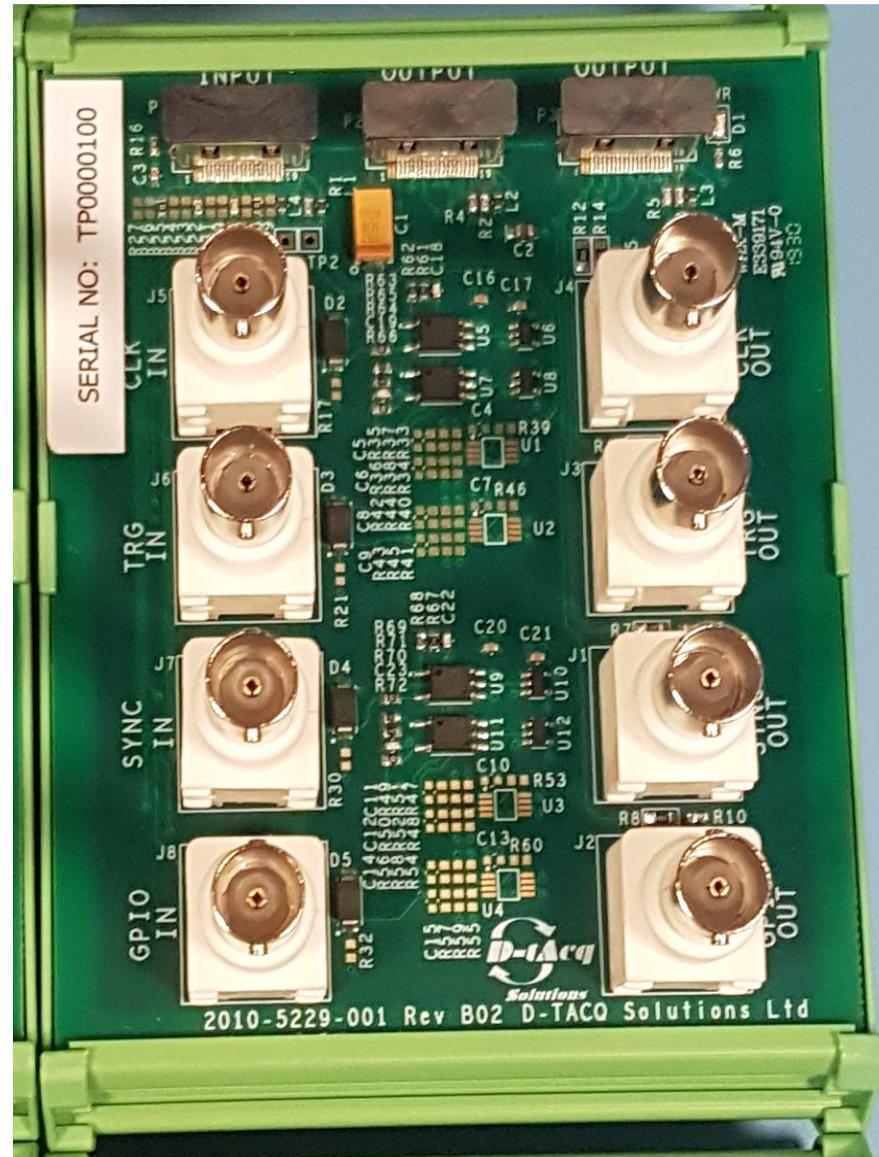


# TERM10 User guide



# Wiring diagram

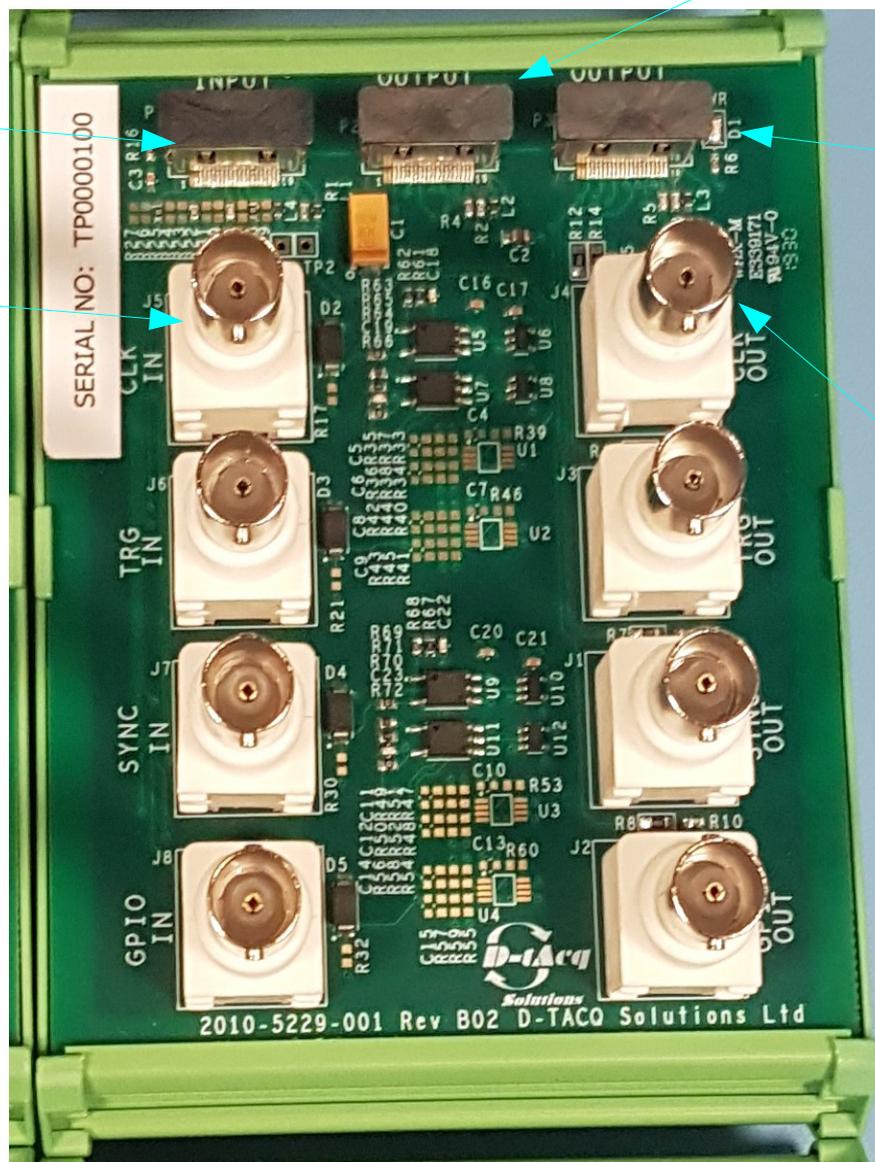
Connect to carrier HDMI INPUT connector

Connect desired clock on CLK IN

Connect to carrier HDMI OUT connector

Optional. Use as a master output if using slave systems. Connect to slave HDMI IN.

Modified clock output visible on CLK OUT



# Additions to sync\_role

A new option to sync\_role has been added to work alongside the term10 – rpmaster. This allows the system to be a master system, clocked from the rear panel, rather than from the front or from the internal clock.

The command can be used as such:

```
acq1001_349> set.site 0 sync_role rpmaster 200k
```

or

```
acq1001_349> set.site 0 sync_role rpmaster 2M
```

# Before using rpmaster command

Here is the configuration of the system before using the rpmaster command. Note – this system has a

```
set.site 0 sync_role master 200000  
command in rc.user.
```

The screenshot displays the CS-Studio interface for configuring the ACQ1001 clock tree and counters. The left pane shows the 'ACQ1001 acq1001\_349 CLOCKTREE' diagram, and the right pane shows the 'ACQ1001 acq1001\_349 SYNC' and 'acq1001\_349 COUNTERS' configuration panels.

**ACQ1001 acq1001\_349 CLOCKTREE**

The clock tree diagram shows the following components and connections:

- XCLK** and **FPLEMO** are inputs to the **OFF** block.
- OFF** outputs **XCLK** and **FCLK** to the **EXT** block.
- EXT** outputs **ZCLK** to the **INT33M** block.
- INT33M** outputs **CLK.d0** through **CLK.d7**.
- ZCLK** is also an input to the **MBCLK** block.
- MBCLK** is the main clock source, receiving **3.333E7** Hz from **EXT** and **2E7** Hz from **MBCLK SETPOINT**.
- MBCLK** outputs **HDMI-CLK** to the **FXI** and **MCLK** blocks.
- FXI** outputs **HDMI** and **GPG0** signals, with a frequency of **3.333E7** Hz.
- MCLK** outputs **HDMI** and **GPG1** signals, with a frequency of **2.000E7** Hz.
- INT01M** is another input to the **FXI** block.
- DIVIDE** is a parameter for the clock tree.

**ACQ1001 acq1001\_349 SYNC**

The sync configuration panel includes the following sections:

- Main Timing Highway Source Routing**:

	d0	d1
CLK	EXT	MCLK
TRG	EXT	STRIG
SYNC	EXT	EXT
- HDMISync Out Select**:

	CLK	d2
CLK	CLK	d2
TRG	TRG	d2
SYNC	SYNC	d2
- EXT SYNC BUS OUT [HDMI]**:

	CLK	TRG	SYNC	GPIO
CABLE PRESENT	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
- Event Bus Source**:

	d0	d1	d2	d3	d4	d5	d6	d7
TRG								

**acq1001\_349 COUNTERS**

The counter configuration panel shows the following data:

CLK.d0	CLK.d1	CLK.d2	CLK.d3
3.333E7 Hz	2.000E7 Hz	2.000E5 Hz	0.000 Hz
1E10	8E9	1E8	0
EXT <input checked="" type="checkbox"/>	MB <input checked="" type="checkbox"/>	S1 <input checked="" type="checkbox"/>	S2 <input checked="" type="checkbox"/>
TRG.d0	TRG.d1	TRG.d2	TRG.d3
0.000 Hz	0.000 Hz	0.000 Hz	0.000 Hz
0	0	0	0
EXT <input checked="" type="checkbox"/>	MB <input checked="" type="checkbox"/>	S1 <input checked="" type="checkbox"/>	S2 <input checked="" type="checkbox"/>
EVT.d0	EVT.d1	EVT.d2	EVT.d3
0.000 Hz	0.000 Hz	0.000 Hz	0.000 Hz

# Using rpmaster command

Here is the configuration of the same system immediately after using:  
`set.site 0 sync_role rpmaster 200k`

The screenshot displays the CS-Studio interface for configuring the ACQ1001 clocktree and sync components. The main window shows the ACQ1001 acq1001\_349 CLOCKTREE configuration, which includes a clock tree diagram with inputs like XCLK, FPLEMO, and ZCLK, and outputs like MBCLK, HDMI-CLK, and MCLK. The Master Site configuration is set to CLK, external, d1, rising, clkdiv 100, and 2.000E5. The ACQ1001 acq1001\_349 SYNC configuration shows the Main Timing Highway Source Routing, HDMI Sync Out Select, and EXT SYNC BUS OUT [HDMI] settings. The Event Bus Source configuration is also visible. The ACQ1001\_349 COUNTERS configuration shows the CLK.d0, CLK.d1, CLK.d2, and CLK.d3 counters, along with TRG.d0, TRG.d1, TRG.d2, and TRG.d3 triggers, and EVT.d0, EVT.d1, EVT.d2, and EVT.d3 events.

CLK.d0	CLK.d1	CLK.d2	CLK.d3
1.000E6 Hz	2.000E7 Hz	2.000E5 Hz	0.000 Hz
1E8	1E9	2E7	0
EXT	MB	S1	S2

TRG.d0	TRG.d1	TRG.d2	TRG.d3
1.000 Hz	0.000 Hz	0.000 Hz	0.000 Hz
67	0	0	0
EXT	MB	S1	S2

EVT.d0	EVT.d1	EVT.d2	EVT.d3
1.000 Hz	0.000 Hz	0.000 Hz	0.000 Hz

# Example rpmaster commands

sync\_role can now take any clock parameter passed to it. For example (and demonstration purposes only as acq423 max clock speed is 200k) here is rpmaster with an argument of 2M.

```
set.site 0 sync_role rpmaster 2M
```

The screenshot displays the CS-Studio interface for configuring the ACQ1001 clock tree and counters. The left pane shows the 'ACQ1001 acq1001\_349 CLOCKTREE' diagram, and the right pane shows the 'ACQ1001 acq1001\_349 SYNC' and 'acq1001\_349 COUNTERS5' configuration panels.

**ACQ1001 acq1001\_349 CLOCKTREE**

The clock tree diagram shows the following components and connections:

- Inputs:** XCLK, FPLEMO, ZCLK, INT33M.
- Logic:** OFF, XCLK, FPCLK, ZCLK, EXT, MBCLK, INT01M, MCLK, GPG0, GPG1, DIVIDE.
- Outputs:** d0, d1.
- Registers:** MBCLK FIN (1E6), MBCLK SETPOINT (2E7).
- Master Site:** CLK (external), d1, rising, clkdiv (10), 2.000E6.

**ACQ1001 acq1001\_349 SYNC**

The sync configuration panel includes the following sections:

- Main Timing Highway Source Routing:** d0, d1. CLK: HDMI, MCLK; TRG: HDMI, STRIG; SYNC: HDMI, EXT.
- HDMISync Out Select:** CLK: CLK, d2; TRG: TRG, d2; SYNC: SYNC, d2; GPIO: DO, d0.
- EXT SYNC BUS OUT [HDMI]:** CABLE PRESENT, CLK, TRG, SYNC, GPIO.
- Event Bus Source:** d0-d7. TRG: TRG, TRG, TRG, TRG, TRG, TRG, TRG, TRG.

**acq1001\_349 COUNTERS5**

CLK.d0	CLK.d1	CLK.d2	CLK.d3
1.000E6 Hz	2.000E7 Hz	2.000E6 Hz	0.000 Hz
1E7	2E8	3E7	0
EXT	MB	S1	S2
TRG.d0	TRG.d1	TRG.d2	TRG.d3
1.000 Hz	0.000 Hz	0.000 Hz	0.000 Hz
13	0	0	0
EXT	MB	S1	S2
EVT.d0	EVT.d1	EVT.d2	EVT.d3
1.000 Hz	0.000 Hz	0.000 Hz	0.000 Hz

# Scope trace of input and output from TERM10.

Here is the scope trace of the signal generator clock input on C3 (orange trace) and the d0 (EXT clock) output from the TERM10 on C4 (purple trace). The phase difference is approximately 80ns. Please note that the 'rpmaster' command does NOT set this routing. To check this you will have to manually set the clock output selection to d0.



# Scope trace of input and output from TERM10.

Here is the scope trace of the signal generator clock input on C3 (orange trace) and the d1 (MBCCLK) output from the TERM10 on C4 (purple trace).

